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Title:	SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME		
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Docket No.:	GK0012RI		

CERTIFICATE OF TRANSLATION OF FOREIGN PRIORITY DOCUMENT UNDER 37 C.F.R. § 1.55(a)

Attached hereto as Exhibit A is an English language translation of Korean Patent Application 1999-18244, which was filed in Korea on May 20, 1999. I, the undersigned, hereby certify that the English language translation attached as Exhibit A is an accurate translation of Korean patent Application 1999-18244.

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1999-18244

TITLE: SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING THE SAME

[ABSTRACT]

Disclosed is an ultra-slim semiconductor package having excellent heat radiation properties and a method for manufacturing the same. The semiconductor package includes a semiconductor chip having a first surface, a second surface, and a number of input/output pads formed on the second surface; a circuit board having a resin layer, a circuit pattern layer, a cover coat layer, and a through-hole, the resin having first and second surfaces, the circuit pattern layer including a number of ball lands formed on the first surface of the resin layer and a number of bond fingers formed on the second surface of the resin layer, the ball lands and the bond fingers being connected to each other by conductive via-holes, the cover coat layer covering the circuit pattern layer while exposing the bond fingers and the ball lands, the through-hole being formed at the center of the circuit board, and the semiconductor chip being positioned in the through-hole; electrical connection means for electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board; a sealant partially enclosing the semiconductor chip, the connection means, and the circuit board; and a number of

conductive balls melted and attached to the ball lands of the circuit board.

[REPRESENTATIVE FIGURE]

FIG. 1

[SPECIFICATION]

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIGs. 1 to 5 are sectional views showing a semiconductor package according to the present invention;

FIGs. 6a to 6f show a series of steps of a method for manufacturing a semiconductor package according to the present invention, respectively; and

FIG. 7 is a sectional view showing a semiconductor package according to the prior art.

[BRIEF DESCRIPTION OF REFERENCE NUMERALS]

2: semiconductor chip

2a: first surface of semiconductor chip

2b: second surface of semiconductor chip

4: input/output pad

6: connection means

10: circuit board

11: resin layer

11a: first surface of circuit board

11b: second surface of circuit board

12: bond finger

14: conductive via-hole

15: ball land

16: cover coat

17: dam

18: through-hole

20: sealant

30: conductive ball

C: closing member

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[RELATED FIELD OF THE INVENTION AND PRIOR ART]

The present invention relates to a semiconductor package and a method for manufacturing the same, and more particularly to an ultra-slim semiconductor package having excellent heat radiation performance and a method for manufacturing the same.

Recent semiconductor packages tend to be compact and slim, as in the case of BGA (ball grid array) semiconductor packages, chip-scale semiconductor packages, and micro-BGA semiconductor packages.

In addition, semiconductor chips mounted on the semiconductor packages generate an increasing amount of heat during operation, because, as a result of improvement in integration technology and manufacturing equipment, power circuits have better performance, operating frequency increases, and circuit functions become more complicated.

FIG. 7 shows a conventional BGA semiconductor package.

The package has a semiconductor chip 1' positioned at the center thereof with a number of electronic circuits integrated thereon. The semiconductor chip 1' has an input/output pad 2' formed on a surface thereof. The center of an upper surface of a PCB 10' is attached to the bottom surface of the semiconductor chip 1' with an adhesive 3' interposed between them.

The PCB 10' has a resin layer 15' positioned at the center thereof, a circuit pattern layer formed on top of the resin layer 15', and a number of ball lands 13' formed beneath the resin layer 15'. The circuit pattern layer includes a bond finger 11' and a connector 12', which are positioned on the outer peripheral edge of the semiconductor chip 1'. The bond finger 11', the connector 12', and the ball lands 13' are made of a conductive material, such as copper. The connector 12' is connected to the ball lands 13' by conductive via-holes 14'. The upper and lower surfaces of the resin layer 15' are coated

with a cover coat 16', except the bond finger 11' and the ball lands 13', to protect the circuit pattern layer from external environments.

The input/output pad 2' of the semiconductor chip 1' is connected to the bond finger 11' on the upper surface of the PCB 10' via a conductive wire 4'. The upper surface of the PCB 10' is sealed with a sealant 20' to protect the semiconductor chip 1' and the conductive wire 4' from external environments.

The ball lands 13' on the bottom surface of the PCB 10' are mounted on a motherboard (not shown) with a number of conductive balls 40' melted thereon, in order to mediate a predetermined electrical signal between the semiconductor chip 1' and the motherboard.

The semiconductor chip 1' of the BGA semiconductor package exchange electrical signals with the motherboard via the input/output pad 2', conductive wire 4', bond finger 11', connector 12', via-holes 14', ball lands 13', and conductive balls 40'.

However, conventional BGA semiconductor packages, constructed as above, have a problem in that, since a semiconductor chip is attached to the upper surface of a thick PCB, the overall thickness of the packages inevitably increases. This is contrary to current trends towards compactness and slimness, as mentioned above. As a result,

they are not applicable to recent ultra-slim electronic devices, including portable telephones, cellular phones, and wireless pagers.

In addition, conventional BGA semiconductor packages are not equipped proper heat radiation means, although their semiconductor chips generate an increasing amount of heat. This degrades the overall performance of the semiconductor chips. In a worse case, the semiconductor chips may stop functioning and, as a result, the semiconductor packages or electronic devices incorporating them may stop operating.

In an attempt to facilitate heat radiation from semiconductor chips to the exterior, some semiconductor packages have a heat radiation plate mounted thereon. However, this further increases the thickness of the semiconductor packages, as well as the manufacturing cost.

[TECHNICAL OBJECT TO ACHIEVE]

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide an ultra-slim semiconductor package and a method for manufacturing the same.

Another object of the present invention is to provide a semiconductor package capable of efficiently radiating heat

from its semiconductor chip to the exterior and a method for manufacturing the same.

[CONSTRUCTION AND OPERATION OF THE INVENTION]

In order to accomplish these objects, there is provided a semiconductor package including a semiconductor chip having a first surface, a second surface, and a number of input/output pads formed on the second surface; a circuit board having a resin layer, a circuit pattern layer, a cover coat layer, and a through-hole, the resin having first and second surfaces, the circuit pattern layer including a number of ball lands formed on the first surface of the resin layer and a number of bond fingers formed on the second surface of the resin layer, the ball lands and the bond fingers being connected to each other by conductive via-holes, the cover coat layer covering the circuit pattern layer while exposing the bond fingers and the ball lands, the through-hole being formed at the center of the circuit board, and the semiconductor chip being positioned in the through-hole; electrical connection means for electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board; a sealant partially enclosing the semiconductor chip, the connection means, and the circuit board; and a number of conductive balls melted and attached to the ball lands of the circuit board.

Preferably, the second surface of the semiconductor chip faces the same direction that a surface of the circuit board having the bond fingers formed thereon faces, and the first surface of the semiconductor chip, a surface of the circuit board having the ball lands formed thereon, and a surface of the sealant are flush with one another.

Preferably, the sealant is formed on an entire surface of the circuit board having the bond fingers formed thereon.

The ball lands may also be formed on a surface of the circuit board having the bond fingers formed thereon.

The conductive balls may be melted and attached to the ball lands on the surface of the circuit board having the bond fingers formed thereon.

The semiconductor chip may have a closing member attached to the first surface thereof to cover the through-hole of the circuit board.

The closing member may be insulating tape.

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor package including the steps of providing a strip-shaped circuit board having a resin layer, a number of bond fingers formed on an upper surface of the resin layer, a number of ball lands formed on a bottom surface of the resin layer, and a number of through-holes formed on the circuit board, the bond fingers and

the ball lands being connected to each other by conductive via-holes; positioning a number of semiconductor chips in the respective through-holes of the circuit board, the semiconductor chips having a number of input/output pads formed on an upper surface thereof; electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board; sealing predetermined regions of the semiconductor chip, connection means, and the circuit board with a sealant; melting and attaching conductive balls to the ball lands of the circuit board to form input/output terminals; and subjecting the circuit board to singulation to obtain separate semiconductor packages.

Preferably, the method further includes a step of attaching a through-hole closing member to a surface of the circuit board having the ball lands formed thereon, before the step of positioning a number of semiconductor chips in the respective through-holes of the circuit board.

Preferably, the closing member is removed, before the step of melting and attaching conductive balls to the ball lands of the circuit board to form input/output terminals, after the step of melting and attaching conductive balls to the ball lands of the circuit board to form input/output terminals, or after the step of subjecting the circuit board to singulation.

The closing member is preferably insulating tape, and more preferably UV tape. The closing member may be a copper layer having excellent thermal conductivity.

In the step of sealing, the sealant may be formed on an entire surface of the circuit board having the bond fingers formed thereon. In this case, the sealant and the circuit board are subjected to singulation together.

In the step of providing a strip-shaped circuit board, a number of ball lands may be additionally formed on a surface of the circuit board having the bond fingers formed thereon. In this case, a number of conductive balls may be additionally melted and attached to the ball lands on the surface of the circuit board having the bond fingers formed thereon.

The semiconductor package and method for manufacturing the same according to the present invention are advantageous in that, since a through-hole is formed in a predetermined area on the circuit board and a semiconductor chip is positioned in the through-hole, the thickness of the semiconductor chip is counterbalanced by the thickness of the circuit board. This makes it possible to manufacture an ultra-slim semiconductor package.

In addition, a surface of the semiconductor package is directly exposed to the exterior to facilitate heat radiation

from the semiconductor chip into the air. This improves the thermal and electrical performance of the semiconductor chip.

Furthermore, a surface of the circuit board is entirely sealed with a sealant to prevent the circuit board from bending.

A preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

FIGs. 1 to 5 are sectional views showing a semiconductor package according to the present invention.

Referring to FIG. 1, a semiconductor chip 2 has first and second surfaces 2a and 2b formed on the lower and upper portions thereof, respectively. A number of input/output pads 4 are positioned on the second surface 2b.

The semiconductor chip 2 is positioned within a through-hole 18, which is formed on a circuit board 10 at a predetermined size. The through-hole 18 has an area larger than that of the first or second surface 2a or 2b of the semiconductor chip 2. The circuit board 10 includes a resin layer 11 having first and second surfaces 11a and 11b positioned on the lower and upper portions thereof, respectively; a through-hole 18, in which the semiconductor chip 2 is positioned; a number of conductive circuit pattern layers, including ball lands 15, formed on the first surface

11a of the resin layer 11 outside the through-hole 18; and a number of conductive circuit pattern layers, including bond fingers 12, formed on the second surface 11b of the resin layer 11 while being electrically connected to the circuit pattern layers on the first surface 11a by conductive via-holes 14.

The bond fingers 12 are preferably plated with gold (Au) or silver (Ag) to promote easy bonding to connection means 6 at a later time. The ball lands 15 are preferably plated with gold (Au), silver (Ag), nickel (Ni), or palladium (Pd) to promote easy bonding to conductive balls 30 later. The resin layer 11 is preferably made of BT (bismaleimide triazine) epoxy resin having enough hardness.

The conductive circuit pattern layers are coated with a cover coat 16 to protect them from external physical, chemical, electrical, or mechanical impact, except the bond fingers 12 and the ball lands 15. The cover coat 16 is generally made of a high-molecular resin having insulating properties.

The input/output pads 4 of the semiconductor chip 2 are electrically connected to the bond fingers 12 of the circuit pattern layers by conductive connection means 6. The conductive connection means 6 may be conductive wires made of gold (Au) or aluminum (Al). Alternatively, the conductive connection means 6 may be leads extending from the bond fingers 12.

The semiconductor chip 2 and the connection means 6 are sealed with a sealant 20 to protect them from external physical, chemical, or mechanical impact. The sealant 20 may span the entire upper surface of the circuit board 10, as shown in FIG. 1, to prevent the circuit board from bending. Alternatively, the sealant 20 may seal parts of the circuit board 10, on which the semiconductor chip 2, connection means 6, and bond fingers 12 are positioned, as shown in FIG. 2. The sealant 20 may be an epoxy molding compound, which is applied using a mold, as shown in FIGs. 1 and 2. Alternatively, the sealant 20 may be a liquid sealant, which is applied by a dispenser, as shown in FIG. 3. Preferably, the circuit board 10 has a dam 17 formed on the upper surface thereof to prevent the liquid sealant from flowing to the exterior during a sealing process. The liquid sealant may also be used for the semiconductor package shown in FIG. However, use of the liquid sealant is not limited to that in the present invention.

The second surface 2b of the semiconductor chip 2 faces the same direction that the surface of the circuit board 10, on which the bond fingers 12 are positioned, faces. The first surface 1a of the semiconductor chip 2, the surface of the circuit board 10 on which the ball lands 15 are positioned, and a surface of the sealant 20 are flush with one another for slimness of the semiconductor package. The first surface 2a of

the semiconductor chip 2 is exposed to the exterior of the sealant 20 to facilitate heat radiation from the semiconductor chip 2 to the exterior.

A number of conductive balls 30, which are made of tin (Sn), lead (Pb), or an alloy thereof, are melted and attached to the ball lands 15, which are formed on the circuit pattern layers of the circuit board 10 on the first surface 11a of the resin layer 11, to be mounted on a motherboard later.

A number of ball lands 15 may be additionally formed on the circuit pattern layers on the second surface 11b of the resin layer 11, as shown in FIG. 4. The ball lands 15 are not covered with the cover coat 16 so that a number of semiconductor packages can be stacked thereon later. Particularly, a number of conductive balls 30 are additionally melted and attached to the ball lands 15 on the second surface 11b of the resin layer 11, as shown in FIG. 5, so that a number of semiconductor packages can be stacked thereon.

The semiconductor package shown in FIGs. 1 to 4 may have a closing member (not shown) attached to the entire first surface 2a of the semiconductor chip 2, as well as to the entire through-hole 18. Preferably, the closing member is insulating tape for protecting the first surface 2a of the semiconductor chip 2. Alternatively, the closing member may be a copper

layer for improving the rate of heat radiation from the semiconductor chip 2.

A method for manufacturing a semiconductor package according to the present invention will now be described with reference to FIGs. 6a to 6f, which show a series of steps thereof, respectively.

A strip-shaped circuit board 10 is provided, which includes a resin layer 11 having first and second surfaces 11a and 11b. The resin layer 11 has an enough number of through-holes 18 formed thereon to position a semiconductor chip 2, which has first and second surfaces 2a and 2b, thereon. The circuit board 10 includes a number of circuit pattern layers formed thereon, including a number of ball lands 15 formed on the first surface 11a and a number of bond fingers 12 formed on the second surface 11b. The circuit pattern layers on the first surface 11a are connected to those on the second surface 11b by conductive via-holes 14. The circuit pattern layers are coated with a cover coat layer 16 while exposing the bond fingers 12 and the ball lands 15 (FIG. 6a).

The circuit board 10 may additionally have a number of ball lands 15 on the second surface 11b of the resin layer 11, on which the bond finger 12 are formed, and a cover coat layer 16 may be formed on the circuit board 10 while exposing the ball lands 15.

The semiconductor chip 2 is positioned within the through-holes 18 of the circuit board 10 in such a manner that input/output pads 4 of the semiconductor chip 2 face the same direction that the surface of the circuit board 10, on which the bond fingers 12 are positioned, faces.

A closing member C is attached to the bottom surface of the through-holes 18 of the circuit board 10 in advance while covering them. Then, the first surface 2a of the semiconductor chip 2 is positioned on the closing member C.

The through-hole closing member C is preferably insulating tape, more preferably UV tape, which is easily peeled off by heat or UV rays (FIG. 6b).

The input/output pads 4 of the semiconductor chip 2 are electrically connected to the bond fingers 12 of the circuit board 10 by connection means 6, which may be conductive wires (e.g. gold wires or aluminum wires) or leads (not shown) extending from the bond fingers 12 (FIG. 6c).

The semiconductor chip 2 and connection means 6 on the upper surface of the closing member C, as well as the entire upper surface of the circuit board 10 are sealed with a sealant 20, which may be an epoxy molding compound or a liquid sealant. Alternatively, only limited regions of the semiconductor chip 2, connection means 6, and circuit board 10 may be sealed with

the sealant 20, which can be easily selected by those skilled in the art (FIG. 6d).

A number of conductive balls 30 are melted and attached to the ball lands 15, which are formed on the bottom surface of the circuit board 10, to be mounted on a motherboard later (FIG. 6e). When ball lands 15 are also formed on the upper surface of the circuit board 10, on which the bond fingers 12 are formed, corresponding conductive balls 30 are melted and attached to the ball lands 15 so that a number of semiconductor packages can be stacked thereon later.

Various methods may be used to melt and attach the conductive balls 30. However, a screen printing method is preferred. In particular, the ball lands 15 of the circuit board 10 are dotted with sticky fluxes, conductive balls 30 are temporarily attached to the fluxes, and the circuit board 10 is put into a furnace so that the conductive balls 30 are melted and attached to the ball lands 15.

Finally, the circuit board 10 is divided into separate semiconductor packages using a singulation tool 70 (FIG. 6f).

Preferably, the closing member C is removed to expose the first surface 2a of the semiconductor chip 2 to the exterior, before the step of melting and attaching conductive balls 30 to the ball lands 15 of the circuit board 10 to form input/output terminals, after the step of melting and attaching conductive

balls 30 to form input/output terminals, or after the singulation step.

When the entire upper surface of the circuit board 10 is sealed with the sealant 20, the sealant 20 and the circuit board 10 are subjected to singulation together to obtain a semiconductor package as shown in FIG. 1.

Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

[EFFECT OF THE INVENTION]

The semiconductor package and method for manufacturing the same according to the present invention are advantageous in that, since a through-hole is formed in a predetermined area on the circuit board and a semiconductor chip is positioned in the through-hole, the thickness of the semiconductor chip is counterbalanced by the thickness of the circuit board. This makes it possible to manufacture an ultra-slim semiconductor package.

In addition, a surface of the semiconductor package is directly exposed to the exterior to facilitate heat radiation

from the semiconductor chip into the air. This improves the thermal and electrical performance of the semiconductor chip.

Furthermore, a surface of the circuit board is entirely sealed with a sealant to prevent the circuit board from bending.

(57) CLAIMS

1. A semiconductor package comprising:

a semiconductor chip having a first surface, a second surface, and a number of input/output pads formed on the second surface;

a circuit board having a resin layer, a circuit pattern layer, a cover coat layer, and a through-hole, the resin having first and second surfaces, the circuit pattern layer including a number of ball lands formed on the first surface of the resin layer and a number of bond fingers formed on the second surface of the resin layer, the ball lands and the bond fingers being connected to each other by conductive via-holes, the cover coat layer covering the circuit pattern layer while exposing the bond fingers and the ball lands, the through-hole being formed at the center of the circuit board, and the semiconductor chip being positioned in the through-hole;

electrical connection means for electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board;

a sealant partially enclosing the semiconductor chip, the connection means, and the circuit board; and

a number of conductive balls melted and attached to the ball lands of the circuit board.

2. The semiconductor package as claimed in claim 1, wherein the second surface of the semiconductor chip faces the same direction that a surface of the circuit board having the bond fingers formed thereon faces, and the first surface of the semiconductor chip, a surface of the circuit board having the ball lands formed thereon, and a surface of the sealant are flush with one another.

3. The semiconductor package as claimed in claim 1 or 2, wherein the sealant is formed on an entire surface of the circuit board having the bond fingers formed thereon.

4. The semiconductor package as claimed in claim 1 or 2, wherein the ball lands are also formed on a surface of the circuit board having the bond fingers formed thereon.

5. The semiconductor package as claimed in claim 4, wherein the conductive balls are melted and attached to the ball lands on the surface of the circuit board having the bond fingers formed thereon.

6. The semiconductor package as claimed in claim 1, wherein the semiconductor chip has a closing member attached to the first surface thereof to cover the through-hole of the circuit board.

7. The semiconductor package as claimed in claim 6, wherein the closing member is insulating tape.

8. The semiconductor package as claimed in claim 6, wherein the closing member is a copper layer.

9. A method for manufacturing a semiconductor package comprising the steps of:

providing a strip-shaped circuit board having a resin layer, a number of bond fingers formed on an upper surface of the resin layer, a number of ball lands formed on a bottom surface of the resin layer, and a number of through-holes formed on the circuit board, the bond fingers and the ball lands being connected to each other by conductive via-holes;

positioning a number of semiconductor chips in the respective through-holes of the circuit board, the semiconductor chips having a number of input/output pads formed on an upper surface thereof;

electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board;

sealing predetermined regions of the semiconductor chip, connection means, and the circuit board with a sealant;

melting and attaching conductive balls to the ball lands of the circuit board to form input/output terminals; and

subjecting the circuit board to singulation to obtain separate semiconductor packages.

10. The method for manufacturing a semiconductor package as claimed in claim 9, further comprising a step of attaching a through-hole closing member to a surface of the circuit board having the ball lands formed thereon, before the step of positioning a number of semiconductor chips in the respective through-holes of the circuit board.

11. The method for manufacturing a semiconductor package as claimed in claim 10, wherein the closing member is removed, before the step of melting and attaching conductive balls to the ball lands of the circuit board to form input/output

terminals, after the step of melting and attaching conductive balls to the ball lands of the circuit board to form input/output terminals, or after the step of subjecting the circuit board to singulation.

12. The method for manufacturing a semiconductor package as claimed in claim 10 or 11, wherein the closing member is insulating tape.

13. The method for manufacturing a semiconductor package as claimed in claim 12, wherein the insulating tape is UV tape.

14. The method for manufacturing a semiconductor package as claimed in claim 10 or 11, wherein the closing member is a copper layer.

15. The method for manufacturing a semiconductor package as claimed in claim 9, wherein, in the step of sealing, the sealant is formed on an entire surface of the circuit board having the bond fingers formed thereon.

16. The method for manufacturing a semiconductor package as claimed in claim 9, wherein, in the step of subjecting the

circuit board to singulation, the sealant and the circuit board are subjected to singulation together.

17. The method for manufacturing a semiconductor package as claimed in claim 9, wherein, in the step of providing a strip-shaped circuit board, a number of ball lands are additionally formed on a surface of the circuit board having the bond fingers formed thereon.

18. The method for manufacturing a semiconductor package as claimed in claim 17, wherein, in the step of melting and attaching conductive balls, a number of conductive balls are additionally melted and attached to the ball lands on the surface of the circuit board having the bond fingers formed thereon.

FIG.1

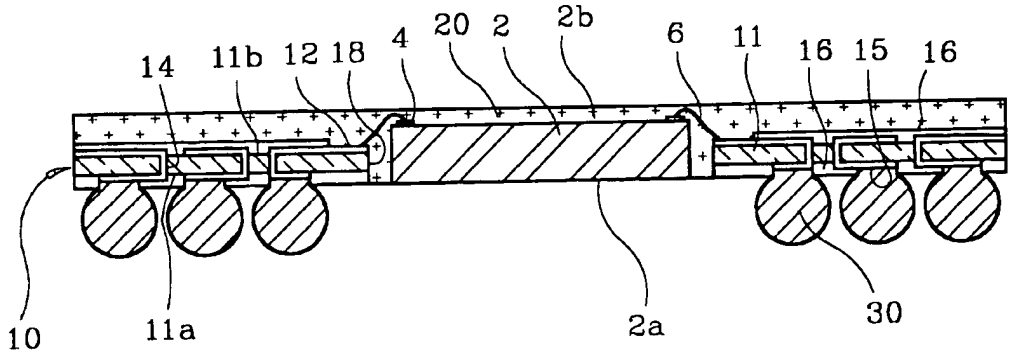

FIG.2

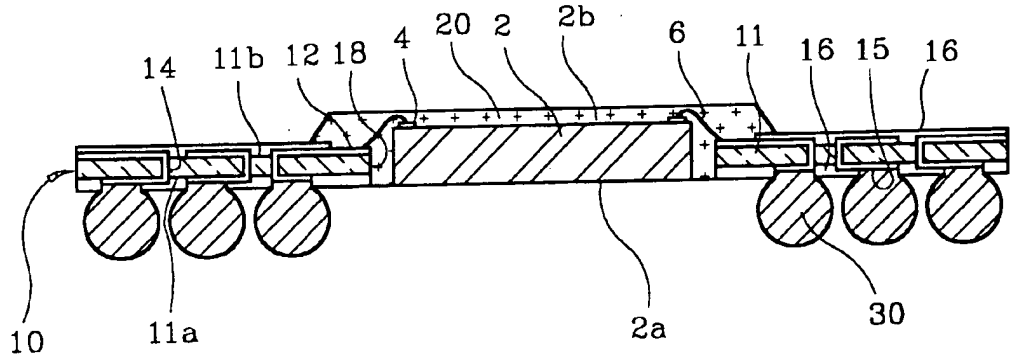

FIG.3

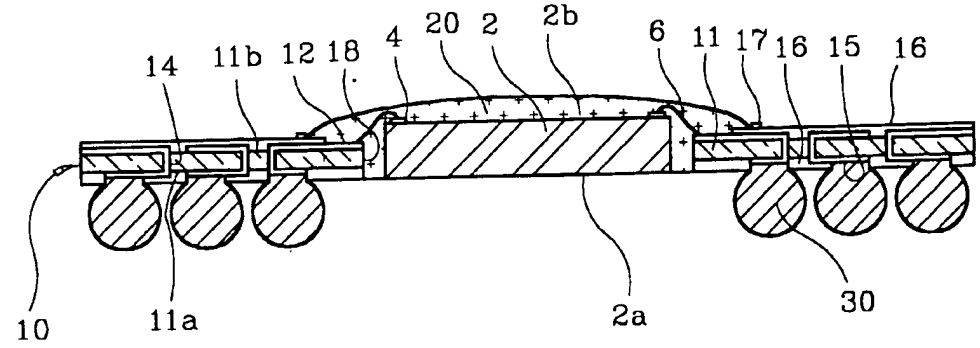

FIG.4

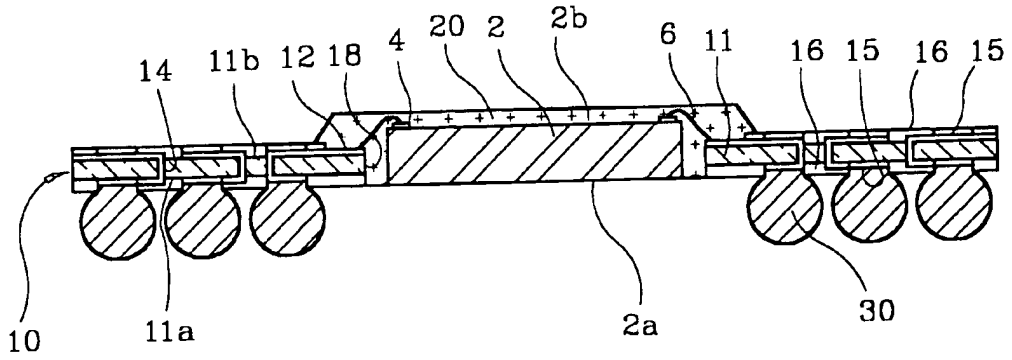
14
11b
12
18
4
20
2
2b
6
11
16
15
16
15
10
11a
2a
30

FIG.5

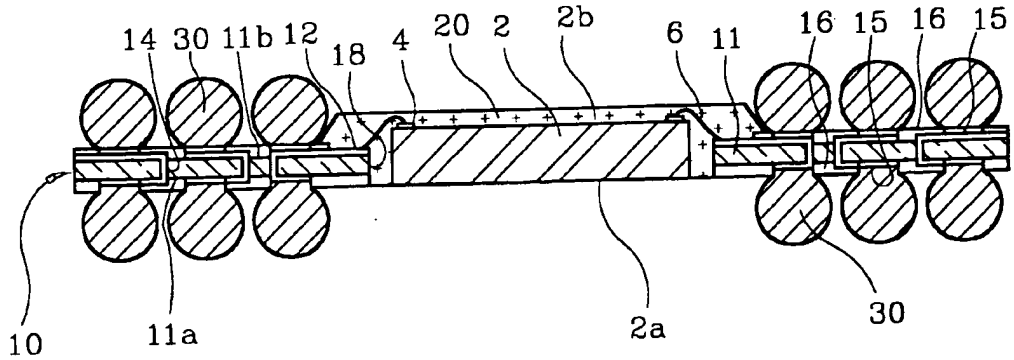
14
30
11b
12
18
4
20
2
2b
6
11
16
15
16
15
10
11a
2a
30

FIG.6a

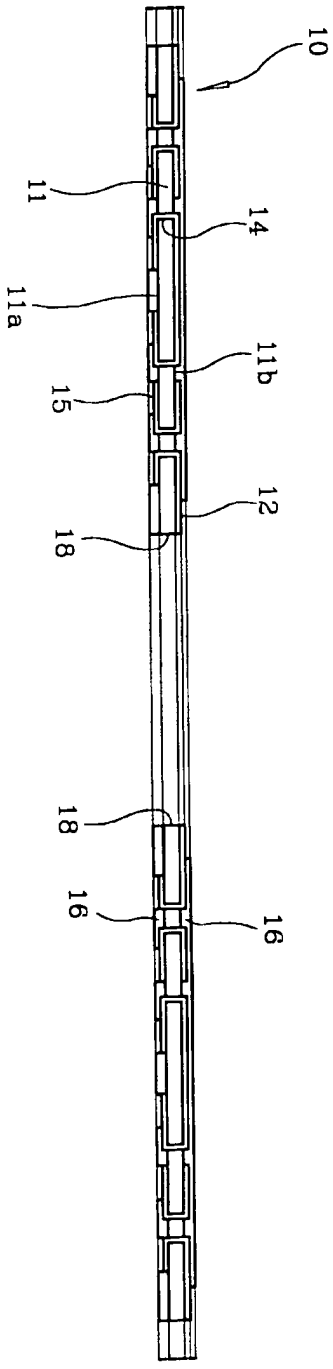

FIG.6b

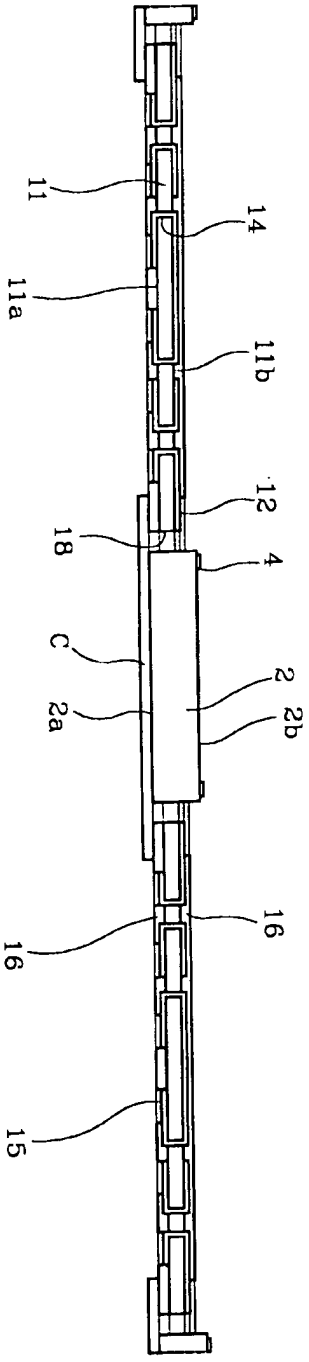

FIG.6c

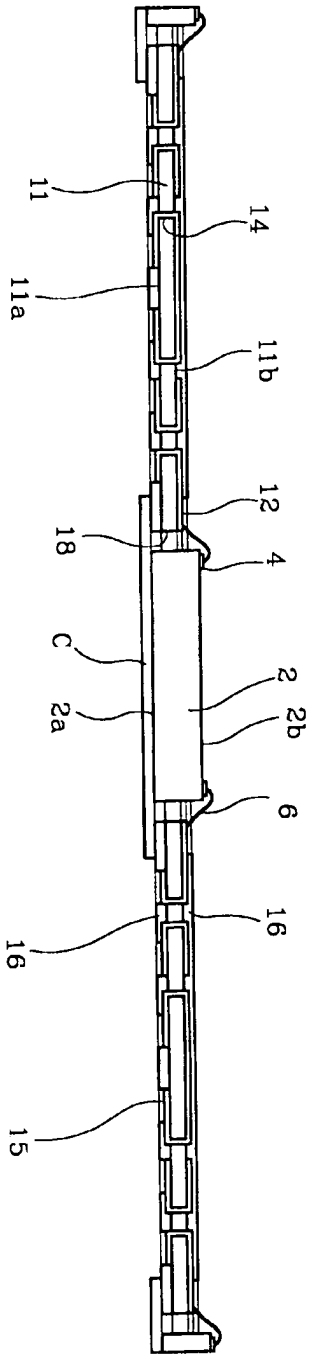

FIG.6d

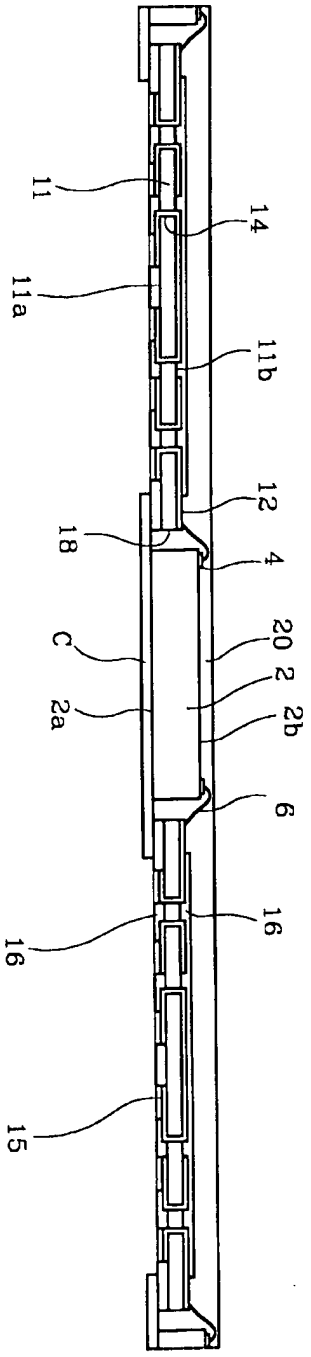

FIG.6e

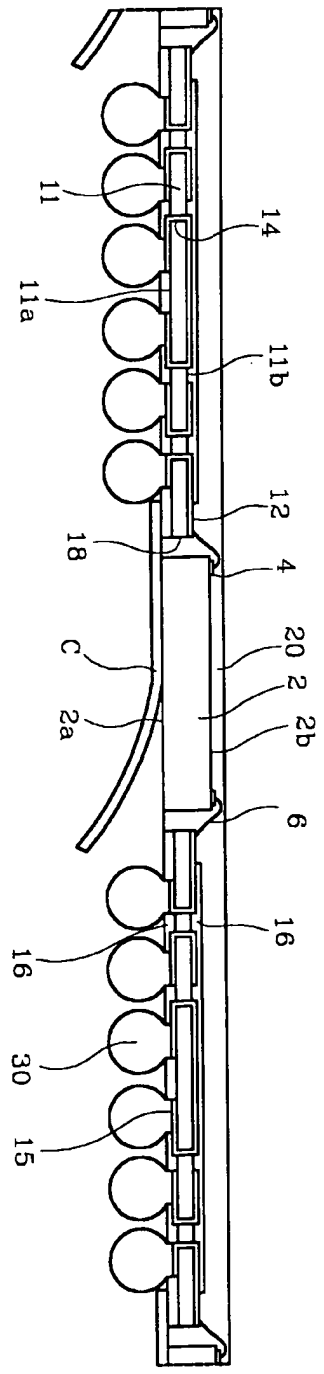

FIG.6f

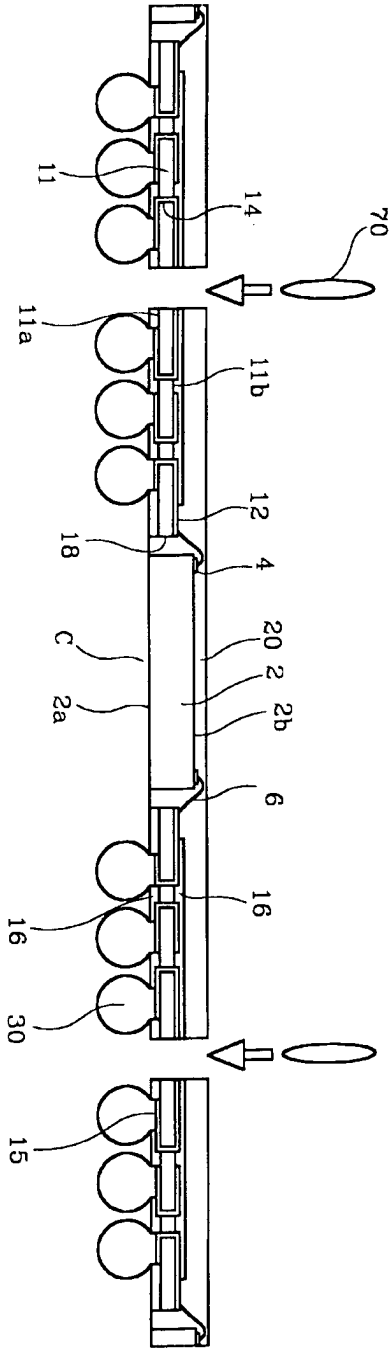

FIG.7